UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/725,463	11/30/2000	Masashi Ogawa	PF-2702/NEC/US/mh	9448

466 7590 10/04/2004

YOUNG & THOMPSON
745 SOUTH 23RD STREET
2ND FLOOR
ARLINGTON, VA 22202

EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/725,463	OGAWA ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-113* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-113* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 November 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 11-338922.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/13/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-116 were examined.

Drawings

2. The drawings are objected to because figure 24 drawing code number 72; the word "informations" does not exist. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Information Disclosure Statement

3. The listing of references in the specification (pg.2, lines 7-16) is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Claim Interpretation

4. Office personnel are to give claims their **"broadest reasonable interpretation"** in light of the supporting disclosure. *In re Morris,* 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. *In re Prater,* 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551(CCPA 1969). See *also *In re Zletz,* 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322(Fed. Cir. 1989) ("During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow") .... The reason is simply that during patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed .... An essential purpose of patent examination is to fashion claims that are precise, clear, correct, and unambiguous. Only in this way can uncertainties of claim scope be removed, as much as possible, during the administrative process. The examiner did not

consider the steps outlined in the method claims since there's a Japanese national standard of testing integrated circuits. Subsequently, the examiner equates "power model" and power source (i.e., V_{dd}, V_{source}, etc.).

Specification

5. 35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms, which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or **verbose** terms used in the specification are: The disclosure of "power current" for example on page 4, lines 14-15 is misleading, for example. The examiner assumes the statements should read "power and current" or voltages and currents since power is derived from voltage squared divided by resistance. Subsequently, the examiner assumes the statement of "first and second power" is first and second power **sources**. Furthermore, "informations" is not a word.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

7. Regarding claims 21, 22,32, 35,38,41,46,47,52,57,60,66,64,71,72,81,85,91 the word "utilize" renders the claims indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

8. Regarding claims 71-98, the word "system" renders the claims vague and indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

9. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The technical terms "semiconductor integrated circuit" are unclear and redundant since and integrated circuits are semiconductors.

10. Furthermore, regarding claims 3,21,27,32,35,38,52,57,60,66,63,71,72,77,82,85,88, and 91, the word "informations" is objected to because no such word exists. Appropriate correction is required.

Claim Rejections - 35 USC § 103

11. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1-116 are rejected under 35 U.S.C. 103 (a) as unpatentable by the Standard of Electronic Industries Association of Japan (EIAJ ED-5302 (1998)) in view of Jyu et al. (U.S. Patent (1999)). The EIAJ standardizes the electronic model of input an output signal, power supply and ground terminal of integrated circuits (IC) in order to provide for analysis of electronic characteristics of equipment using them (pg.1, section 2, Scope), as well as accurately predict electrical, via simulation (e.g., SPICE software program), performance to include noise in electronic systems with IC; but doesn't provide an examples with inversion

capabilities, timing concerns etc. Jyu et al teaches a method for minizing signal delays and power consumption through simulation and delay analysis (abstract).

At the time the invention, it would have been obvious to one of ordinary skill in the art to use Jyu et al. to modify EAIJ since it would be advantageous negate as much circuitry signal delay as much as possible during simulation.

Claim 1. A power model for a semiconductor integrated circuit (EIAJ: pg. 4, table 4.1 with pgs 2 and 3) wherein said power model comprises a logic gate circuit part representing an operating part of said semiconductor integrated circuit (EIAJ: pg. 13, part (vi), MOS transistor; and pg. 19, part (ii), MOS Transistor Model) and an equivalent internal capacitive part representing (Jyu: column 28, lines 10-14) a non-operating part of said semiconductor integrated circuit.

Claim 2. The power model as claimed in claim 1, (EIAJ: pg. 4, table 4.1 with pgs 2 and 3; Jyu: column 28, lines 10-14) wherein said power model is independently provided for each of plural power systems (EIAJ: pg. 14, parts (vii)-(xiii)), which are independent from each other and included in said semiconductor integrated circuit.

Claim 3. The power model as claimed in claim 1, (EIAJ: pg. 4, table 4.1 with pgs 2 and 3; Jyu: column 28, lines 10-14) wherein internal circuit configurations of said semiconductor integrated circuit are divided into plural blocks on the basis of

arrangement information, and said power model is provided for each of said plural blocks (EIAJ: pg.11, section 5.2.5 with pg.38, figure 8.2).

Claim 4. The power model as claimed in claim 1, (EIAJ: pg. 4, table 4.1 with pgs 2 and 3; Jyu: column 28, lines 10-14) wherein internal circuit configurations of said semiconductor integrated circuit are divided into plural groups (EIAJ: pg.11, section 5.2.5 with pg.38, figure 8.2), each of said plural groups comprises a same timing group which includes logic gate circuits having individual signal transmission delay times (Jyu: column 7, lines 1-11) fallen in a group-belonging predetermined time range which belongs to each of said plural groups, and said power model is provided for each of said plural groups (EIAJ: pg.11, section 5.2.5 with pg.38, figure 8.2)

Claim 5. The power model as claimed in claim 1, (EIAJ: pg. 4, table 4.1 with pgs 2 and 3; Jyu: column 28, lines 10-14) wherein said power model further comprises a signal source connected to said logic gate circuit part for supplying a frequency-fixed signal (Jyu: column 7, lines 1-11) to said logic gate circuit part, so that said logic gate circuit part represents operating state parts of said semiconductor integrated circuit in accordance with said frequency-fixed signal (EIAJ: pg. 14, part (xiii), PULSE; Jyu: column 2, lines 6-18) and said equivalent

internal capacitive part represents non-operating state parts of said semiconductor integrated circuit (EIAJ: pg.11, section 5.2.5).

Claim 6. The power model as claimed in claim 5, (EIAJ: pg. 4, table 4.1 with pgs 2 and 3; Jyu: column 28, lines 10-14) wherein said equivalent internal capacitive part further represents operating irrelevant fixed parts of said semiconductor integrated circuit (EIAJ: pg.11, section 5.2.5 with pg.38, figure 8.2).

Claim 7. The power model as claimed in claim 6, (EIAJ: pg. 4, table 4.1 with pgs 2 and 3; Jyu: column 28, lines 10-14) wherein said logic gate circuit part is connected between first and second powers (EIAJ: pg. 16, figure 5.3, V_{cc2} and $V_{cc3,}$) and said equivalent internal capacitive part (Jyu: column 29, lines 6-49) connected between said first and second powers.

Claim 8. The power model as claimed in claim 7, (EIAJ: pg. 4, table 4.1 with pgs 2 and 3; Jyu: column 28, lines 10-14) wherein said logic gate circuit part further comprises a single pair of an inverter circuit and a load capacitive element, and said inverter circuit (Jyu: column, lines 27, 25-33) is connected between said first and second powers and said load capacitive element is also connected between said first and second powers (EIAJ: pg. 16, figure 5.3, V_{cc2} and $V_{cc3,}$) and said load

capacitive element is placed between said inverter circuit and said equivalent internal capacitive part (Jyu: column 28, lines 10-14).

Claim 9. The power model as claimed in claim 8, (EIAJ: pg. 4, table 4.1 with pgs 2 and 3; Jyu: column 28, lines 10-14) wherein said load capacitive element comprises a series connection of a first load capacitance and a second load capacitance between (Jyu: column 28, lines 60-66; with column 29, lines 1-49) said first and second powers (EIAJ: pg. 16, figure 5.3, V_{cc2} and V_{cc3},), and an intermediate point between said first and second load capacitances is connected to an output terminal of said inverter circuit (Jyu: column 30-33).

Claim 10. The power model as claimed in claim 9, (EIAJ: pg. 4, table 4.1 with pgs 2 and 3; Jyu: column 28, lines 10-14) wherein said equivalent internal capacitive (Jyu: column 28, lines 10-14) part further comprises at least an equivalent internal capacitive element connected between said first and second powers (EIAJ: pg. 16, figure 5.3, V_{cc2} and V_{cc3},).

Claim 11. The power model as claimed in claim 10, (EIAJ: pg. 4, table 4.1 with pgs 2 and 3; Jyu: column 28, lines 10-14) wherein a plurality of said equivalent internal capacitive element (Jyu: column 28, lines 10-14) is connected between said first and second powers, and said equivalent internal capacitive element

comprises a series connection of a capacitance and a resistance between said first and second powers (EIAJ: pg. 16, figure 5.3, V_{cc2} and V_{cc3},).

Claim 12. The power model as claimed in claim 11, (EIAJ: pg. 4, table 4.1 with pgs 2 and 3; Jyu: column 28, lines 10-14) wherein said inverter circuit comprises a series connection of a p-channel MOS field effect transistor and an n-channel MOS field effect transistor, and gate electrodes of said p-channel and n-channel MOS field effect transistors (Jyu: table 2) are connected to a clock signal (Jyu: column 2, lines 6-10) source for applying a clock signal to said gate electrodes of said p-channel and n-channel MOS field effect transistors.

Claim 13. The power model as claimed in claim 7, (EIAJ: pg. 4, table 4.1 with pgs 2 and 3; Jyu: column 28, lines 10-14) wherein said logic gate circuit part further comprises plural pairs of an inverter circuit (Jyu: column 27, lines 25-32) and a load capacitive element, and said inverter circuit (Jyu: column 27, lines 25-32) is connected between said first and second powers (EIAJ: pg. 16, figure 5.3, V_{cc2} and V_{cc3}) and said load capacitive element is also connected between said first and second powers, and in each pair, said load capacitive clement is placed closer to said equivalent internal capacitive part than said inverter circuit (Jyu: column 27, lines 25-32).

Claim 14. The power model as claimed in claim 13, (EIAJ: pg. 4, table 4.1 with pgs 2 and 3; Jyu: column 28, lines 10-14) wherein said load capacitive element comprises a series connection of a first load capacitance (Jyu: column 28, lines 10-14) and a second load capacitance between said first and second powers (EIAJ: pg. 16, figure 5.3, V_{cc2} and V_{cc3}), and an intermediate point between said first and second load capacitances is connected to an output terminal of said inverter circuit (Jyu: column 27, lines 25-32).

Claim 15. The power model as claimed in claim 14, (EIAJ: pg. 4, table 4.1 with pgs 2 and 3; Jyu: column 28, lines 10-14) wherein said equivalent internal capacitive part (Muriai: column 5, lines 35-40) further comprises at least an equivalent internal capacitive element connected between said first and second powers.

Claim 16. The power model as claimed in claim 15, (EIAJ: pg. 4, table 4.1 with pgs 2 and 3; Jyu: column 28, lines 10-14) wherein a plurality of said equivalent internal capacitive element is connected between said first and second powers, and said equivalent internal capacitive element comprises a series connection of a capacitance and a resistance between said first and second powers.

Claim 17. The power model as claimed in claim 16, (EIAJ: pg. 4, table 4.1 with pgs 2 and 3; Jyu: column 28, lines 10-14) wherein said inverter circuit comprises a series connection of a p-channel MOS field effect transistor and an n-channel MOS field effect transistor, and gate electrodes of said p-channel and n-channel MOS field effect transistors (Jyu: column 9, table 2) are connected to a clock signal (Jyu: column 2, lines 6-10) source for applying a clock to said gate electrodes of said p-channel and n-channel MOS field effect transistors.

Claim 18. The power model as claimed in claim 1, (EIAJ: pg. 4, table 4.1 with pgs 2 and 3; Jyu: column 28, lines 10-14) wherein said equivalent internal capacitive part (Jyu: column 28, lines 10-14) is placed between said logic gate circuit part and a power system side.

Claim 19. The power model as claimed in claim 1, (EIAJ: pg. 4, table 4.1 with pgs 2 and 3; Jyu: column 28, lines 10-14) wherein said power model is deigned for simulation (EIAJ: pg. 1, Background) to a current distribution (Jyu: column 7, lines 5-11) over a circuit board on which said semiconductor integrated circuit is mounted.

Claim 20. The power model as claimed in claim 19, (EIAJ: pg. 4, table 4.1 with pgs 2 and 3; Jyu: column 28, lines 10-14) wherein said power model isdeigned for an electromag

Claim 21.A method of designing a power model for a semiconductor integrated circuit (EIAJ: operating-related information of all gate circuits constituting said semiconductor integrated circuit (Jyu: column 9, table 2; EIAJ: pg. 5 and 6) are utilized in first sequential processes to prepare said logic gate circuit part of said power model, (Jyu: figure 6, sub-numbers 602-612 with column 13, 46-61) and wherein non-operating-related information of said all gate circuits constituting said semiconductor integrated circuit are utilized in second sequential processes separated from said first sequential processes to prepare said equivalent internal capacitive part of said power model.

Claim 22. The method as claimed in claim 21(EIAJ: pg.1, Background, pg. 2, Outline: Jyu: abstract), wherein, in said first sequential processes (Jyu: figure 6, sub-numbers 602-612 with column 13, 46-61), information about gate widths of operating-state p-channel transistors in said operating-state of said constituting gate circuits are utilized to decide a gate width of a model p-channel transistor (EIAJ: pg. 6, Circuit Description); information about gate widths (EAIJ: pg. 13, part (vi)) of operating-state n-channel transistors in said operating-state of said constituting gate circuits are utilized to decide a gate width of a model n-channel transistor (Jyu: column 9, table 2, parameter 4); informations about gate capacities of said operating-state p-channel (Jyu: column 9, table 2, parameter 5) transistors in said operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state p-channel transistors and a first power

are utilized to decide a model first load capacity; and informations about gate capacities of said operating-state n-channel transistors (Jyu: column 9, table 2, parameter 4) in said operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state n-channel transistors and a second power are utilized to decide a model second load capacity, whereby said logic gate circuit part comprising at least a pair of p-channel and n-channel transistors and at least a pair of first and second load capacities is designed (EIAJ: PG. 6, Circuit Description; pg.19, part, (ii)).

Claim 23. The method as claimed in claim 22, (EIAJ: pg.1, Background, pg. 2, Outline: Jyu: abstract) wherein a sum of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor (EIAJ: PG. 6, Circuit Description; pg. 13, part (vi); pg.19, part, (ii)); a sum of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor (EIAJ: PG. 6, Circuit Description; pg.19, part, (ii); pg. 20-21, Junction Diode Characteristics; and pg. 13, part (vi)); a sum of gate capacitances of said operating-state p-channel transistors and interconnection capacitances between said operating-state p-channel transistors and said first power is defined to be a model first load capacity (EIAJ: pg. 6, Circuit Description; pg.19, part, (ii); pg. 20-21, Junction Diode Characteristics; pg. 6, * number of inner terminal/outer

terminals); and a sum of gate capacitances of said operating-state n-channel transistors and interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity, whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed (EIAJ: PG. 6, Circuit Description; pg.19, part, (ii); pg. 20-21, Junction Diode Characteristics; pg. 6, * number of inner terminal/outer terminals).

Claim 24. The method as claimed in claim 22, (EIAJ: pg.1, Background, pg. 2, Outline: Jyu: abstract) wherein a half of a sum of gate widths of said operating-state p-channel transistors (Jyu: column 13, lines 62-67) in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor; a half of a sum of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor (EIAJ: PG. 6, Circuit Description; pg.19, part, (ii); pg. 20-21, Junction Diode Characteristics; pg. 6, * number of inner terminal/outer terminals); a half of a sum of gate capacitances of said operating-state p-channel transistors and interconnection capacitances between (EIAJ: pg. 19, part (ii)) said operating-state p-channel transistors and said first power is defined to be a model first load capacity; and a half of a sum of gate capacitances of said operating-state n-channel transistors and

interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity, whereby said logic gate circuit part comprising two pairs (EIAJ: pg. 19, part (ii)) of p-channel and n-channel transistors and two pairs of first and second load capacities is designed.

Claim 25. The method as claimed in claim 22, (EIAJ: pg.1, Background, pg. 2, Outline: Jyu: abstract) wherein a product of the number of said operating-state gate circuits and an averaged value of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor (Jyu: column 9, table 2, parameter 5); a product of the number of said operating-state gate circuits and an averaged value of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width (EIAJ: pg. 19, part (ii)) of a model n-channel transistor (Jyu: column 9, table 2, parameter 4); a product of the number of said operating-state gate circuits and a sum of both a first averaged value of gate capacitances of said operating-state p-channel transistors and a second averaged value of interconnection capacitances between said operating-state p-channel transistors and said first power is defined to be a model first load capacity; and a product of the number of said operating-state gate circuits and a sum of both a first averaged value of gate capacitances of said operating-state n-channel transistors (Jyu: column 9, table

2, parameter 4) and a second averaged value of interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity, whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed.

Claim 26. The method as claimed in claim 22, (EIAJ: pg.1, Background, pg. 2, Outline: Jyu: abstract) wherein a half of a product of the number of said operating-state gate circuits and an averaged value of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width (EIAJ: pg. 19, part (ii)) of a model p-channel transistor (Jyu: column 9, table 2, parameter 5); a half of a product of the number of said operating-state gate circuits and an averaged value of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor (Jyu: column 9, table 2, parameter 4); a half of a product of the number of said operating-state gate circuits and a sum of both a first averaged value of gate capacitances of said operating-state p-channel transistors and a second averaged value of interconnection capacitances between said operating-state p-channel transistors and said first power is defined to be a model first load capacity (Jyu: column 25, lines 1-11); and a half of a product of the number of said operating-state gate circuits and a sum of both a first averaged value (Jyu:

column 25, lines 1-18) of gate capacitances of said operating-state n-channel transistors and a second averaged value of interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity, whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors (Jyu: column 9, table 2) and two pairs of first and second load capacities is designed.

Claim 27. The method as claimed in claim 21, (EIAJ: pg.1, Background, pg. 2, Outline: Jyu: abstract) wherein, in said first sequential processes, informations about gate widths of all p-channel transistors of said constituting gate circuits and an information about operational rate of operating-state p-channel transistors in said operating-state are utilized to decide a gate width (EIAJ: pg. 19, part (ii)) of a model p-channel transistor; informations about gate widths of all n-channel transistors (Jyu: column 9, table 2, parameter 4) of said constituting gate circuits and an information about operational rate of operating-state n-channel transistors in said operating-state are utilized to decide a gate width (EIAJ: pg. 19, part (ii))of a model n-channel transistor; informations about gate capacities of said all p-channel transistors of said constituting gate circuits (Jyu: column 9, table 2, parameter 5) and informations about interconnection capacitances between said all p-channel transistors (Jyu: column 9, table 2, parameter 5) and a first power and informations about said operational rate are utilized to do a model first load

capacity and informations about gate capacities of said all n-channel transistors of said constituting gate circuits and informations about interconnection capacitances between said all n-channel transistors and a second power and informations about said operational rate are utilized to decide a model second load capacity, whereby said logic gate circuit part comprising at least a pair of p-channel and n-channel transistors and at least a pair of first and second load capacities is designed (EAIJ: pg.19, part (ii)) through pg. 21).

Claim 28. The method as claimed in claim 27, (EIAJ: pg.1, Background, pg. 2, Outline: Jyu: abstract) wherein a product of the number of said all gate circuits, an average operational rate of said gate circuits (Jyu: column 25, lines 1-20), and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor; a product of the number of said all gate circuits, an average operational rate of said gate circuits (Jyu: column 25, lines 1-20), and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor); a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors (Jyu: column 9, table 2, parameter 5) and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity (Jyu: column 25, lines 1-20); and

a product of the number of said all gate circuits, an average operational rate of said gate circuits (Jyu: column 25, lines 1-20), and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity, whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed (Jyu: column 25, lines 1-20).

Claim 29. The method as claimed in claim 27, (EIAJ: pg.1, Background, pg. 2, Outline: Jyu: abstract) wherein a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor (EAIJ: pg.19, part (ii)) through pg. 21); a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor (columns 13 and 14, lines 65-67; 1-4); a half of a product of the number of said all gate circuits, an average operational rate (Jyu: column 25, lines 1-18) of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances

between said all p-channel transistors and said first power is defined to be a model first load capacity; and a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value (Jyu: column 25, lines 1-20) of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity, whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors (Jyu: columns 13 and 14, lines 65-67; 1-4) and two pairs of first and second load capacities is designed.

Claim 30. The method as claimed in claim 27, (EIAJ: pg.1, Background, pg. 2, Outline: Jyu: abstract) wherein a product of the number of said all gate circuits, a maximum operational rate of said gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor (Jyu: columns 13 and 14, lines 65-67; 1-4); a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor; a product of the number of said all gate circuits (Jyu: column 28, lines 40-41), said maximum operational

rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity (Jyu: column 14, table 5); and a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity (Jyu: column 25, lines 1-12), whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed

Claim 31. The method as claimed in claim 27, (EIAJ: pg.1, Background, pg. 2, Outline: Jyu: abstract) wherein a half of a product of the number of said all gate circuits, a maximum operational rate of said gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor; a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate (Jyu: column 25, lines 1-18); a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all

p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity (Jyu: column 9, table 2; column 11, lines 3-11); and a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity (Jyu: columns 13 and 14, lines 65-67; 1-4), whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed

Claim 32. The method as claimed in claim 21, (EIAJ: pg.1, Background, pg. 2, Outline: Jyu: abstract) wherein, in said first sequential processes, informations about gate widths of all p-channel transistors of said constituting gate circuits and informations (Jyu: column 11, lines 35-39) about currents of basic gate circuits and said constituting gate circuits are utilized to decide a gate width of a model p-channel transistor (EIAJ: pg. 19, part (ii); Jyu: column 9, table 2; column 11, lines 3-11); informations about gate widths of all n-channel transistors of said constituting gate circuits and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide a gate width of a model

n-channel transistor (EIAJ: pg. 19, part (ii); Jyu: column 9, table 2; column 11, lines 3-11); informations about gate capacities of said all p-channel transistors of said constituting gate circuits and informations about interconnection capacitances between said all p-channel transistors and a first power and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide a model first load capacity (EIAJ: pg. 19, part (ii);Jyu: column 9, table 2; column 11, lines 3-11); and informations about gate capacities of said all n-channel transistors of said constituting gate circuits and informations about interconnection capacitances between said all n-channel transistors and a second power and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide a model second load capacity, whereby said logic gate circuit part comprising at least a pair of p-channel and n-channel transistors and at least a pair of first and second load capacities is designed (EIAJ: pg. 19, part (ii) ;with pg. 20, example and figure 5.5).

Claim 33. The method as claimed in claim 32, (EIAJ: pg.1, Background, pg. 2, Outline: Jyu: abstract) wherein a product of the number of said all gate circuits, and a power current ratio (Jyu: column 17, lines 55-57) of an averaged current value of said basic gate circuits to an averaged current value of said constituting gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor; a product of the number of said all gate circuits,

said power current ratio (Jyu: column 17, lines 55-57), and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor; a product of the number of said all gate circuits, said power current ratio, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity; and a product of the number of said all gate circuits, said power current ratio (Jyu: column 17, lines 55-57), and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity, whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed (Jyu: column 14, lines 65-67; column 13 and 14, lines 65-67 and 1-6).

Claim 34. The method as claimed in claim 32, (EIAJ: pg.1, Background, pg. 2, Outline: Jyu: abstract) wherein a half of a product of the number of said all gate circuits, and a power current ratio (Jyu: column 17, lines 55-57) of an averaged current value of said basic gate circuits to an averaged current value of said constituting gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a

gate width of a model p-channel transistor; a half of a product of the number of said all gate circuits, said power current ratio, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor; a half of a product of the number of said all gate circuits, said, power current ratio, (Jyu: column 17, lines 55-57) and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and power is defined to be a model first load capacity; and a half of a product of the number of said all gate circuits, said power current ratio, (Jyu: column 17, lines 55-57) and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined (Jyu: columns 13 and 14, lines 65-67, 1-11 and 66-67, respectively) to be a model second load capacity, whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed.

Claim 35. The method as claimed in claim 21(EIAJ: pg.1, Background, pg. 2, Outline: Jyu: abstract), wherein, in said second sequential processes (Jyu: column 11, lines 36-40), informations about ON-resistances of non-operating-state

transistors in said non-operating-state of said constituting gate circuits (Jyu: column 1, lines 50-55) are utilized to decide an ON-resistance of an equivalent internal capacity; and informations about gate capacities of said non-operating-state transistors (Jyu: figure 6, sub-numbers 602-612 with column 13, 46-61) in said non-operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state transistors and a power (Jyu: column 12, lines 57-58) are utilized to decide said equivalent internal capacity , whereby said equivalent internal capacitive (Jyu: column 28, lines 11-14) part comprising at least said equivalent internal capacity is designed.

Claim 36. The method as claimed in claim 35, (EIAJ: pg.1, Background, pg. 2, Outline: Jyu: abstract) wherein a double of a reciprocal of a sum of reciprocals of ON-resistances of non-operating p-channel transistors in said non-operating state is defined to be an ON-resistance of a third equivalent internal capacity; a double of a reciprocal of a sum of reciprocals of ON-resistances of non-operating n-channel transistors in said non-operating state is defined to be an ON-resistance of a second equivalent internal capacity (Jyu: column 28, lines 10-14); an arithmetic mean of a sum of gate capacities of said non-operating p-channel transistors and a sum of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity; and an arithmetic mean of a sum of gate capacities of said non-operating n-channel (EIAJ: pg. 19, part (ii); Jyu: column 9, table 2; column

11, lines 3-11) transistors and a sum of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity, whereby said equivalent internal capacitive part: comprising at least said equivalent internal capacity is designed.

Claim 37. The method as claimed in claim 35, (EIAJ: pg.1, Background, pg. 2, Outline: Jyu: abstract) wherein a double of a product of an averaged value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity; a double of a product of an averaged value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity; a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating p-channel transistors and an averaged value of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity (Jyu: column 31, claims 3 (lines 5-8) and claim 8); and a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate (Jyu: column 25, lines 1-11; column 14, lines 60-67) capacities of said non-operating n-channel transistors and an averaged value of interconnection capacities between said non-operating n-channel transistors and a

second power is defined to be said third equivalent internal capacity, whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

Claim 38. The method as claimed in claim 21, (EIAJ: pg.1, Background, pg. 2, Outline: Jyu: abstract) wherein, in said second sequential processes (Jyu: column 11, lines 35-39), informations about an averaged value of ON-resistances of all transistors included in said constituting gate circuits and the number of non-operating gate circuits are utilized to decide an ON-resistance of an equivalent internal capacity; and informations about an averaged value of gate capacities of said non-operating-state (Jyu: figure 6, sub-numbers 602-612 with column 13, 46-61) transistors in said non-operating-state of said constituting gate circuits, and the number of non-operating gate circuits as well as informations about an averaged value of interconnection capacitances between said operating-state transistors and a power are utilized to decide said equivalent internal capacity, whereby said equivalent internal capacitive (Jyu: columns 13 and 14, lines 66-67; and 1-11) part comprising at least said equivalent internal capacity is designed.

Claim 39. The method as claimed in claim 38, (EIAJ: pg.1, Background, pg. 2, Outline: Jyu: abstract) wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of a total number of said constituting

logic gate included in said semiconductor integrated circuit (Jyu: figure 6, sub-numbers 602-612 with column 13, 46-61) and a remainder by subtracting an average operational rate (Jyu: column 25, lines 1-12) from 1;a double of a product of an averaged value (Jyu: column 25, lines 1-12) of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity; a double of a product of an averaged value of ON-resistances of non-operating n-channel transistors (Jyu: column 14, lines 60-67) in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity; a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating p-channel transistors and an averaged value of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity; and a product of said number of said non-operating gate circuit and an arithmetic mean (Jyu: column 14, lines 60-67) of an averaged value of gate capacities of said non-operating n-channel transistors and an averaged value of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity, whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed (Jyu: column 14, lines 60-67).

Claim 40. The method as claimed in claim 38, (EIAJ: pg.1, Background, pg. 2, Outline: Jyu: abstract) wherein the number of non-operating gate circuits (Jyu: figure 6, sub-numbers 602-612 with column 13, 46-61) in said non-operating state is defined to be a product of a total number of said constituting logic gate included in said semiconductor integrated circuit and a remainder by subtracting a maximum operational rate from 1(Jyu: column 14, lines 60-67); a double of a product of an averaged value of ON-resistances of non-operating p-channel transistors (Jyu: columns 13 and 14, lines 65-67; 1-10, respectively) in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity; a double of a product of an averaged (Jyu: column 26, lines 1-12) value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity; a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value (Jyu: column 25, lines 1-10) of gate capacities of said non-operating p-channel transistors and an averaged value of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity (Jyu: column 14, lines 60-67); and a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value (Jyu: column 25, lines 1-10) of gate capacities of said non-operating

n-channel transistors and an averaged value of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity (Jyu: column 22, equations 6 and 7) whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

Claim 41. The method as claimed in claim 21, (EIAJ: pg.1, Background, pg. 2, Outline: Jyu: abstract) wherein informations about an averaged value of ON-resistances of all transistors included in said constituting gate circuits (EIAD: pg. 19, part (ii) through pg. 22) and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide an ON-resistance of an equivalent internal capacity; and informations about an averaged value (Jyu: column, lines 1-11) of gate capacities of said non-operating-state transistors in said non-operating-state of said constituting gate circuits, and informations about currents of basic gate circuits and said constituting gate circuits as well as informations about an averaged value of interconnection capacitances between said operating-state transistors and a power (Jyu: abstract) are utilized to decide said equivalent internal capacity, whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed (Jyu: column 28, lines 9-14).

Claim 42. The method as claimed in claim 41, wherein the number of non-operating gate circuits in said non-operating state (Jyu: figure 6, sub-numbers 602-612 with column 13, 46-61) is defined to be a product of the total number of the constituting gate circuits (Jyu: column 28, line 11) included in the semiconductor integrated circuit and a power current ratio (Jyu: column 17, lines 55-57) which is defined to be a ratio of an averaged current value of all of basic gate circuits to an averaged current (Jyu: column 25, lines 1-11) value of all of the constituting gate circuits; a double of a product (Jyu: column 11, lines 5-11) of an averaged value of ON-resistances of non-operating p-channel transistors (Jyu: column 13 and 14, lines 65-67, lines 1-10) in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity; a double of a product of an averaged value of ON-resistances of non-operating n-channel transistors(Jyu: column 13 and 14, lines 65-67, lines 1-10) in said non-operating state (Jyu: figure 6, sub-numbers 602-612 with column 13, 46-61) and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity ; a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating p-channel transistors and an averaged value of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity; and a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged

value of gate capacities of said non-operating n-channel transistors(Jyu: column 13 and 14, lines 65-67, lines 1-10) and an averaged value of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity, whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

Claim 43. The method as claimed in claim 21, (EIAJ: pg.1, Background, pg. 2, Outline; Jyu: abstract) wherein said equivalent internal capacitive (Jyu: column, lines 10-14) part is placed between said logic gate circuit part and a power system side (EIAJ: pg. 15, figure 5.3).

Claim 44. The method as claimed in claim 21(EIAJ: pg.1, Background, pg. 2, Outline; Jyu: abstract), wherein said power model is deigned for simulation to a current distribution over a circuit board on which said semiconductor integrated circuit is mounted (EIAJ: pg. 11-12, section 5.2.5).

Claim 45. The method as claimed in claim 44, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract) wherein said power model is deigned for an electromagnetic interference simulation (EIAJ: pg. 2, Outline, note 7) to an electromagnetic field distribution over a circuit board on which said semiconductor integrated circuit is mounted.

Claim 46. A storage medium for storing a computer program (Jyu: column 4, lines 1-5 with figure 1) for designing a power model (Jyu: column 18, lines 27 for a semiconductor integrated circuit, and said power model comprising a logic gate circuit part (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract) and an equivalent internal capacitive part, wherein operating-related informations of all gate circuits constituting said semiconductor integrated circuit are utilized in first sequential processes (Jyu: column 11, lines 37-39) to prepare said logic gate circuit part of said power model, and wherein non-operating-related informations (Jyu: figure 6, sub-numbers 602-612 with column 13, 46-61) of said all gate circuits constituting said semiconductor integrated circuit are utilized in second sequential processes (Jyu: column 11, lines 37-39) separated from said first sequential processes to prepare said equivalent internal capacitive part of said power model.

Claim 47. The storage medium as claimed in claim 46 (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39), wherein, in said first sequential processes, informations about gate widths of operating-state p-channel transistors in said operating-state of said constituting gate circuits are utilized to decide a gate width of a model p-channel transistor; informations about gate widths (EAIJ: pg. 13, part (vi)) of operating-state n-channel transistors in said operating-state of said

constituting gate circuits are utilized to decide a gate width of a model n-channel transistor (Jyu: columns 13 and 14, lines 65-67 and 1-10); informations about gate capacities of said operating-state p-channel transistors in said operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state p-channel transistors and a first power are utilized to decide a model first load capacity (Jyu: column 9, table 2 with columns 13 and 14, lines 65-67 and 1-10); and informations about gate capacities of said operating-state n-channel transistors in said operating state of said constituting gate circuits and about interconnection capacitances between said operating-state n-channel transistors and a second power are utilized to decide a model second load capacity, whereby said logic gate circuit part comprising at least a pair of p-channel and n-channel transistors and at least a pair of first and second load capacities is designed (Jyu: column 9, table 2 with columns 13 and 14, lines 65-67 and 1-10).

Claim 48.The storage medium as claimed in claim 27, (EIAJ: pg.1, Background, pg. 2, Outline: Jyu: abstract) wherein a sum of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor (Jyu: column 9, table 2 with columns 13 and 14, lines 65-67 and 1-10); a sum of gate widths of operating-state n-channel transistors in said operating-state of said constituting

gate circuits is defined to be a gate width of a model n-channel transistor (Jyu: columns 13 and 14, lines 65-67 and 1-10); a sum of gate capacitances of said operating-state p-channel transistors and interconnection capacitances between said operating-state p-channel transistors and said first power is defined to be a model first load capacity; and a sum of gate capacitances of said operating-state n-channel transistors and interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity (Jyu: column 28, lines 29-35), whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed.

Claim 49. The storage medium as claimed in claim 47(EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39), wherein a half of a sum of gate widths (EAIJ: pg. 13, part (vi)) of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width (EAIJ: pg. 13, part (vi)) of a model p-channel transistor (Jyu: column 9, table 2); a half of a sum of gate widths (EAIJ: pg. 13, part (vi)) of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor (Jyu: column 9, table 2); a half of a sum of gate capacitances of said operating-state p-channel transistors and interconnection capacitances between said operating-state p-channel transistors (Jyu: column 9,

table 2) and said first power is defined to be a model first load capacity; and a half of a sum of gate capacitances of said operating-state n-channel transistors (Jyu: column 9, table 2) and interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity, whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed (Jyu: column 9, table 2 with columns 13 and 14, lines 65-67 and 1-10).

Claim 50. The storage medium as claimed in claim 47 (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39), wherein a product of the number of said operating-state gate circuits (Jyu: column 26, lines 27-28) and an averaged value of gate widths of said operating-state p-channel transistors (Jyu: column 9, table 2) in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor (Jyu: column 9, table 2); a product of the number of said operating-state gate circuits and an averaged value of gate widths (EIAJ: pg. 13, part (vi) of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor (Jyu: column 9, table 2); a product of the number (Jyu: column 26, lines 27-28) of said operating-state gate circuits and a sum of both a first average value of gate capacitances of operating-state p-channel transistors and a second averaged value of interconnection capacitances between said

operating-state p-channel transistors and said first power is defined to be a model first load capacity; and a product of the number(Jyu: column 26, lines 27-28) of said operating-state gate circuits and a sum of both a first averaged value of gate capacitances (Jyu: column 25, lines 1-11 with column 22, lines 35-63) of said operating-state n-channel transistors and a second averaged value of interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity, whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed.

Claim 51. The storage medium as claimed in claim 47 (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39), wherein a half of a product of the number of said operating-state gate circuits and an averaged value of gate widths (Jyu: column 25, lines 1-11 with column 22, lines 35-63) of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor; a half of a product of the number of said operating-state gate circuits and an averaged value of gate widths(Jyu: column 25, lines 1-11 with column 22, lines 35-63) of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor; a half of a product of the number of said operating-state gate circuits and a sum of both a first

averaged value of gate capacitances of said operating-state p-channel transistors(Jyu: column 9, table 2) and a second averaged value of interconnection capacitances between said operating-state p-channel transistors and said first power is defined to be a model first load capacity; and a half of a product of the number of said operating-state gate circuits and a sum of both a first averaged value of gate capacitances of said operating-state n-channel transistors (Jyu: column 25, lines 1-11;column 22, lines 35-63; and column 9, table 9) and a second averaged value of interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity, whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed.

Claim 52. The storage medium as claimed in claim 46, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein, in said first sequential processes, informations about gate widths of all p-channel transistors of said constituting gate circuits and an information about operational rate of operating-state p-channel transistors in said operating-state are utilized to decide a gate width of a model p-channel transistor; informations about gate widths of all n-channel transistors of said constituting gate circuits and an information about operational rate of operating-state n-channel transistors (Jyu: column 25, lines 1-11;column

22, lines 35-63; and column 9, table 9) in said operating-state are utilized to decide a gate width of a model n-channel transistor(Jyu: column 25, lines 1-11;column 22, lines 35-63; and column 9, table 9); informations about gate capacities of said all p-channel transistors (Jyu: column 9, table 9) of said constituting gate circuits and informations about interconnection capacitances between said all p-channel transistors and a first power and informations about said operational rate are utilized to decide a model first load capacity; and informations about gate capacities of said all n-channel transistors (Jyu: column 9, table 9) of said constituting gate circuits and informations about interconnection capacitances between said all n-channel transistors and a second power and informations about said operational rate are utilized to decide a model second load capacity, whereby said logic gate circuit part comprising at least a pair of p-channel and n-channel transistors and at least a pair of first and second load capacities is designed.

Claim 53. The storage medium as claimed in claim 52, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an averaged value of gate widths (Jyu: column 25, lines 1-11 with column 22, lines 35-63) of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor; a

product of the number of said all gate circuits, an average operational rate of said gate circuits (Jyu: column 25, lines 1-11 with column 22, lines 35-63); and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor; a product of the number of said all gate circuits, an average operational rate of said gate circuits (Jyu: column 25, lines 1-11;column 22, lines 35-63; and column 9, table 9), and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity (Jyu: column 25, lines 1-11;column 22, lines 35-63; and column 9, table 9); and a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances (Jyu: column 25, lines 1-11 with column 22, lines 35-63) between said all n-channel transistors and said second power is defined to be a model second load capacity, whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed.

Claim 54. The storage medium as claimed in claim 52, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5

with figure 1; column 11, lines 37-39) wherein a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits (Jyu: column 25, lines 1-11;column 22, lines 35-63; and column 9, table 9), and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor (Jyu: column 25, lines 1-11;column 22, lines 35-63; and column 9, table 9); a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor (Jyu: column 25, lines 1-11;column 22, lines 35-63; and column 9, table 9); a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between (Jyu: column 25, lines 1-11;column 22, lines 35-63; and column 9, table 9) said all p-channel transistors and said first power is defined to be a model first load capacity; and a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits (Jyu: column 25, lines 1-11;column 22, lines 35-63; and column 9, table 9), and a sum (Jyu: column 11, lines 3-25) of both a first averaged value of gate capacitances of said alt n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a

model second load capacity, whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed (Jyu: column 14, lines 60-67).

Claim 55. The storage medium as claimed in claim 52, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein a product of the number of said all gate circuits, a maximum operational rate of said gate circuits, and an averaged value of gate widths of said all p-channel transistors (Jyu: column 25, lines 1-11;column 22, lines 35-63; and column 9, table 9) in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor; a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor (Jyu: column 25, lines 1-11;column 22, lines 35-63; and column 9, table 9); a product of the number of said all gate circuits (Jyu: column 26, lines 25-30), said maximum operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors (Jyu: column 25, lines 1-11;column 22, lines 35-63; and column 9, table 9) and a second averaged value of interconnection capacitances between said all p-channel transistors (Jyu: column 25, lines 1-11) and said first power is defined to be a model first load capacity; and a product of the number of said all gate circuits,

said maximum operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity, whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed (Jyu: column 14, lines 60-67).

Claim 56. The storage medium as claimed in claim 52, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein a half of a product of the number of said all gate circuits, a maximum operational rate of said gate circuits, and an averaged value of gate widths (Jyu: column 25, lines 1-11;column 22, lines 35-63; and column 9, table 9) of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor; a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor (Jyu: column 25, lines 1-11;column 22, lines 35-63; and column 9, table 9); a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a

second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity (Jyu: column 25, lines 1-11;column 22, lines 35-63; and column 9, table 9); and a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances (Jyu: column 26, equation 10) of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity, whereby said logic gate circuit part comprising two pairs of n-channel and n-channel transistors and two pairs of first and second load capacities is designed (Jyu: column 14, lines 60-67).

Claim 57. The storage medium as claimed in claim 46, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein, in said first sequential processes, informations about gate widths of all p-channel transistors of said constituting gate circuits and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide a gate width of a model p-channel transistor; informations about gate widths of all n-channel transistors of said constituting gate circuits and informations about currents of basic gate circuits (EIAJ: pg. 19, part (ii); Jyu: column 9, table 2) and said constituting gate circuits are utilized to decide

a gate width of a model n-channel transistor; informations about gate capacities of said all p-channel transistors (Jyu: column 9, table 2) of said constituting gate circuits and informations about interconnection capacitances between said all p-channel transistors and a first power and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide a model first load capacity (Jyu: column 14, table 5, point 6); and informations about gate capacities of said all n-channel transistors of said constituting gate circuits and informations about interconnection capacitances between said all n-channel transistors and a second power and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide a model second load capacity, whereby said logic gate circuit part comprising at least a pair of p-channel (Jyu: columns 13 and 14, lines 65-67 and 1-10, respectively) and n-channel transistors and at least a pair of first and second load capacities is designed (Jyu: column 14, lines 60-67).

Claim 58. The storage medium as claimed in claim 57, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein a product of the number of said all gate circuits, and a power current ratio (Jyu: column 17, lines 55-58) of an averaged current value of said basic gate circuits to an averaged current value of said constituting gate circuits, and an averaged value of gate widths of said all

p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor; a product of the number of said all gate circuits, said power current ratio, and an averaged value of gate widths (column 1, lines 60-65) of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor; a product of the number of said all gate circuits (Jyu: column 11, 1-10) said power current ratio, and a sum of both a first averaged value of gate capacitances of said all p-channel (Jyu: table 9) transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity; and product of the number of said all gate circuits, said power current ratio, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity, whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed (Jyu: column 14, lines 60-67).

Claim 59. The storage medium as claimed in claim 57, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein a half of a product of the number of

said all gate circuits, and a power current ratio (Jyu: column 17, lines 55-58) of an averaged current value of said basic gate circuits to an averaged current value of said constituting gate circuits, and an averaged value of gate widths of said all p-channel transistors (Jyu: table 9) in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor; a half of a product of the number of said all gate circuits, said power current ratio, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor; a half of a product of the number of said all gate circuits, said power current ratio (Jyu: column 17, lines 55-58), and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity; and a half of a product (Jyu: column 11, lines 1-10) of the number of said all gate circuits, said power current ratio, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity, whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed (Jyu: column 14, lines 60-67)

Claim 60. The storage medium as claimed in claim 46, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein, in said second sequential processes, informations about ON-resistances of non-operating-state transistors (Jyu: figure 6, sub-numbers 602-612 with column 13, 46-61) in said non-operating-state of said constituting gate circuits are utilized to decide an ON-resistance of an equivalent internal capacity (Jyu: column 28, lines 9-35); and informations about gate capacities of said non-operating-state transistors in said on-operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state transistors and a power are utilized to decide said equivalent internal capacity, whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed (Jyu: column 28, lines 9-35).

Claim 61. The storage medium as claimed in claim 60, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein a double of a reciprocal of a sum of reciprocals of ON-resistances of non-operating p-channel transistors in said non-operating state is defined to be an ON-resistance of a third equivalent internal capacity; a double of a reciprocal of a sum of reciprocals of ONT-resistances of non-operating n-channel transistors in said non-operating state is defined to be an ON-resistance of a second equivalent internal capacity;

an arithmetic mean (Jyu: column 25, 1-10) of a sum of gate capacities of said non-operating p-channel transistors and a sum of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity; and an arithmetic mean of a sum of gate capacities of said non-operating n-channel transistors and a sum of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity, whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed (Jyu: column 28, lines 9-35).

Claim 62. The storage medium as claimed in claim 60, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein a double of a product of an averaged value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity; a double of a product of an averaged value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity (Jyu: column 28, lines 9-36 with column 28, lines 9-35); a product of said number (Jyu: column 11,

lines 1-10) of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating p-channel transistors and an averaged value of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity; and a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating n-channel transistors and an averaged value of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity, whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed (Jyu: column 28, lines 9-36 with column 28, lines 9-35) .

Claim 63. The storage medium as claimed in claim 46, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein, in said second sequential processes, informations about an averaged value of ON-resistances of all transistors included (Jyu: table 9) in said constituting gate circuits and the number of non-operating gate circuits are utilized to decide an ON-resistance of an equivalent internal capacity (Jyu: column 28, lines 9-36); and informations about an averaged value of gate capacities of said non-operating-state transistors in said non-operating-state of said constituting gate circuits, and the number of non-operating gate circuits as

well as informations about an averaged value of interconnection capacitances between said operating-state transistors and a power are utilized to decide said equivalent internal capacity, whereby said equivalent internal capacitive (Jyu: column 28, lines 9-36) part comprising at least said equivalent internal capacity is designed.

Claim 64. The storage medium as claimed in claim 63, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of a total number of said constituting logic gate (Jyu: column 11, lines 1-10, with table 4) included in said semiconductor integrated circuit and a remainder by subtracting an average operational rate from 1; a double of a product (Jyu: column 11, lines 1-10, with table 4) of an averaged value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity; a double of a product of an averaged value of ON-resistances of non-operating (Jyu: figure 6, sub-numbers 602-612 with column 13, 46-61) n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity; a product of said number (Jyu: column 11, lines 1-10) of said non-operating gate circuit and an arithmetic mean of an averaged value of

gate capacities of said non-operating p-channel transistors and an averaged value of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity; and a product of said number (Jyu: column 11, lines 1-10) of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating n-channel transistors and an averaged value of interconnection capacities (Jyu: column 21, lines 64-66) between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity, whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

Claim 65. The storage medium as claimed in claim 63, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of a total number of said constituting logic gate included in said semiconductor integrated (Jyu: column 11, lines 1-10) circuit and a remainder by subtracting a maximum operational rate from 1; a double of a product (Jyu: column 11, lines 1-10) of an averaged value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity; a double of a product (Jyu: column 11, lines 1-10) of an averaged value of ON-resistances of non-operating

n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity; a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating p-channel transistors (Jyu: column 11, lines 1-10) and an averaged value of interconnection capacities between said non-operating p-channel transistors (Jyu: table 9) and a first power is defined to be said second equivalent internal capacity ; and a product of said number (Jyu: column 11, lines 1-10) of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating n-channel transistors and an averaged value of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity, whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed (Jyu: column 28, lines 9-36 with column 28, lines 9-35).

Claim 66. The storage medium as claimed in claim 46, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein informations about an averaged value of ON-resistances of all transistors included (Jyu: table 9) in said constituting gate circuits and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide an ON-resistance of an equivalent internal capacity; and informations about an averaged value of gate capacities (Jyu: column

25, lines 1-10) of said non-operating-state transistors in said non-operating-state of said constituting gate circuits, and informations about currents of basic gate circuits (Jyu: table 9) and said constituting gate circuits as well as informations about an averaged value of interconnection capacitances between said operating-state transistors and a power (Jyu: abstract) are utilized to decide said equivalent internal capacity, whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

Claim 67. The storage medium as claimed in claim 66, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of the total number of the constituting gate circuits (Jyu: column 11, lines 1-10) included in the semiconductor integrated circuit and a power current ratio (Jyu: column 17, lines 55-57) which is defined to be a ratio of an averaged current value of all of basic gate circuits to an averaged current value of all of the constituting gate circuits; a double of a product (Jyu: column 11, lines 1-10) of an averaged value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity; a double of a product (Jyu: column 11, lines 1-10) of an averaged value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate

circuit is defined to be an ON-resistance of a second equivalent internal capacity; a product of said number (Jyu: column 11, lines 1-10) of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating p-channel transistors and an averaged value of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity; and a product of said number (Jyu: column 11, lines 1-10) of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating n-channel transistors and an averaged value of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity, whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed (Jyu: column 28, lines 9-36 with column 28, lines 9-35).

Claim 68. The storage medium as claimed in claim 46, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein said equivalent internal capacitive (Jyu: column 21, lines 61-67) part is placed between said logic gate circuit part and a power system side.

Claim 69. The storage medium as claimed in claim 46, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with

figure 1; column 11, lines 37-39) wherein said power model is deigned for simulation to a current distribution (EIAJ: pg. 13, line 12) over a circuit board on which said semiconductor integrated circuit is mounted.

Claim 70. The storage medium as claimed in claim 69, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein said power model is deigned for an electromagnetic interference simulation to an electromagnetic field distribution (EIAJ: pg.2, Outline, part 7) over a circuit board on which said semiconductor integrated circuit is mounted.

Claim 71. A supporting system for designing a power model for a semiconductor integrated circuit, and said power model comprising a logic gate circuit part and an equivalent internal capacitive part, and said supporting system (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) comprising; a data base storing informations of internal circuit configurations; a storage medium for storing informations about circuit elements and interconnections between said circuit elements of said power model as well as for storing a computer program for designing said power model (Jyu: figure 1 with column 5, lines 17-37); a processor being connected to said data base and said storage medium for executing said computer program to prepare said power model (Jyu: figure 1 with column 5, lines

17-48); and an output device being connected to said processor for outputting said power model prepared by said processor (Jyu: column 5, lines 55-59), wherein operating-related informations of all gate circuits constituting said semiconductor integrated circuit are utilized in first sequential processes to prepare said logic gate circuit part of said power model, and wherein non-operating-related informations of said all gate circuits constituting said semiconductor integrated circuit are utilized in second sequential processes separated from said first sequential processes to prepare said equivalent internal capacitive part of said power model (Jyu: figure 6 with column 4, lines 15-18).

Claim 72. The supporting system as claimed in claim 71, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39; figure 1 with column 5, lines 17-37) wherein, in said first sequential processes, informations about gate widths of operating-state p-channel transistors in said operating-state of said constituting gate circuits are utilized to decide a gate width of a model p-channel transistor; informations about gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits are utilized to decide a gate width of a model n-channel transistor (Jyu: table 9; EAIJ: pg. 13, part (vi)); informations about gate capacities (Jyu: table 9) of said operating-state p-channel transistors in said operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state p-channel transistors and a first power are utilized to decide a

model first load capacity; and informations about gate capacities of said operating-state n-channel transistors in said operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state n-channel transistors and a second power are utilized to decide a model second load capacity, whereby said logic gate circuit part comprising at least a pair of p-channel and n-channel transistors and at least a pair of first and second load capacities is designed (Jyu: column 7, table 1 and column 9, table 2).

Claim 73. The supporting system as claimed in claim 52, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein a sum of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor (Jyu: column 28, lines 9-36); a sum of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor; a sum of gate capacitances of said operating-state p-channel transistors and interconnection capacitances between said operating-state p-channel transistors and said first power is defined to be a model first load capacity (Jyu: column 9, table 2. column 28, lines 9-36); and a sum of gate capacitances of said operating-state n-channel transistors and interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity, whereby

said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed (Jyu: column 9, table 2).

Claim 74. The supporting system as claimed in claim 72, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein a half of a sum of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor (Jyu: column 9, table 2); a half of a sum of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width (Jyu: column 9, table 2) of a model n-channel transistor; a half of a sum of gate capacitances (Jyu: column 9, table 2) of said operating-state p-channel transistors and interconnection capacitances between said operating-state p-channel transistors and said first power is defined to be a model first load capacity; and a half of a sum of gate capacitances(Jyu: column 9, table 2 with column 14, lines 60-67)) of said operating-state n-channel transistors and interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity, whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed.

Claim 75. The supporting system as claimed in claim 72, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein a product of the number of said operating-state gate circuits and an averaged value of gate widths (Jyu: column 25, lines 1-11) of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor; a product of the number (Jyu: column 11, lines 1-11) of said operating-state gate circuits and an averaged value of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width (Jyu: column 9, table 2) of a model n-channel transistor; a product of the number (Jyu: column 11, lines 1-11) of said operating-state gate circuits and a sum of both a first averaged value of gate capacitances of said operating-state p-channel transistors and a second averaged value of interconnection capacitances between said operating-state p-channel transistors and said first power is defined to be a model first load capacity (Jyu: column 25, lines 1-10); and a product of the number of said operating-state gate circuits and a sum of both (Jyu: column 11, lines 1-11) a first averaged value of gate capacitances of said operating-state n-channel transistors and a second averaged value of interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity, whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed.

Claim 76. The supporting system medium as claimed in claim 72, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein a half of a product of the number of said operating-state gate circuits and an averaged value of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width (Jyu: column 9, table 2) of a model p-channel transistor; a half of a product of the number of said operating-state gate circuits and an averaged value of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor(Jyu: column 9, table 2); a half of a product of the number of said operating-state gate circuits and a sum of both a first averaged value of gate capacitances of said operating-state p-channel transistors and a second averaged value of interconnection capacitances between said operating-state p-channel transistors and said first power is defined to be a model first load capacity (Jyu: column 25, lines 1-10); and a half of a product of the number of said operating-state gate circuits and a sum of both a first averaged value of gate capacitances of said operating-state n-channel transistors and a second averaged value of interconnection capacitances between said operating-state n-channel transistors and said second power (EIAJ: pg. 16, figure 5.3, V_{cc2} and $V_{cc3,}$) is defined to be a model second load capacity, whereby said logic gate circuit part comprising

two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed.

Claim 77. The supporting system as claimed in claim 71, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein, in said first sequential processes (Jyu: figure 6, sub-numbers 602-612 with column 13, 46-61), informations about gate widths of all p-channel transistors of said constituting gate circuits and an information about operational rate of operating-state p-channel transistors in said operating-state are utilized to decide a gate width of a model p-channel transistor; informations about gate widths of all n-channel transistors of said constituting gate circuits and an information about operational rate of operating-state n-channel transistors in said operating-state are utilized to decide a gate width of a model n-channel transistor (Jyu: column 9, table 2); informations about gate capacities of said all p-channel transistors (Jyu: column 9, table 2)of said constituting gate circuits and informations about interconnection capacitances between said all p-channel transistors and a first power and informations about said operational rate are utilized to decide a model first load capacity; and informations about gate capacities of said all n-channel transistors of said constituting gate circuits (Jyu: column 9, table 2) and informations about interconnection capacitances between said all n-channel transistors and a second power and informations about said operational rate are utilized to decide a model second load capacity, whereby said logic gate circuit part comprising at least

a pair of p-channel and n-channel transistors and at least a pair of first and second load capacities is designed (EIAJ; pgs12-14).

Claim 78.The supporting system as claimed in claim 77, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an averaged value of gate widths of said all p-channel transistors (Jyu: column 25, lines 1-10) in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor; a product of the number of said all gate circuits (Jyu: column 11, lines 1-10), an average operational rate of said gate circuits, and an averaged value of gate widths of all n-channel transistors (Jyu: column 9, table 2) in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor; a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity (Jyu: column 11, lines 1-10 with column 25, lines 1-10) ; and a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors (Jyu: column 11, lines 1-10 with column 25, lines 1-10; and column 9, table 2) and a second averaged

value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity, whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed.

Claim 79. The supporting system as claimed in claim 77, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein a half of a product of the number of said all gate circuits (Jyu: column 9,table 2), an average operational rate of said gate circuits, and an averaged value of gate widths of said all p-channel transistors (Jyu: column 25, lines 1-10) in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor; a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an averaged value of gate widths of all n-channel transistors (Jyu: column 25, lines 1-10 with column 9, table 2) in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor; a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity (Jyu: column 11, lines 1-11 with column 14, lines 60-67); and a half of a product of the number of said all gate circuits, an average

operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity, whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed (Jyu: column 11, lines 1-11 with column 14, lines 60-67).

Claim 80. The supporting system as claimed in claim 77, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein a product of the number of said all gate circuits (Jyu: column 9,table 2), a maximum operational rate of said gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor; a product of the number of said all gate circuits (Jyu: column 11, lines 1-10 with table 4), said maximum operational rate of said gate circuits, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to he a gate width of a model n-channel transistor; a product of the number of said all gate circuits (Jyu: column 11, lines 1-10 with table 4), said maximum operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all

p-channel transistors and said first power is defined to be a model first load capacity; and a product of the number of said all gate circuits (Jyu: column 11, lines 1-10 with table 4 with column 9, table 2), said maximum operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel; transistors and said second power is defined to be a model second load capacity, whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed.

Claim 81. The supporting system as claimed in claim 77, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein a half of a product of the number of said all gate circuits, a maximum operational rate of said gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor; a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width (Jyu: column 11, lines 1-10 with table 4 with column 9, table 2) of a model n-channel transistor; a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first averaged value of

gate capacitances of said all p-channel transistors (Jyu: column 11, lines 1-10 with table 4 with column 9, table 2 and column 25, lines 1-10) and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity; and a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits (Jyu: column 9, table 2), and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors (Jyu: column 11, lines 1-10 with column 9, table 2) and said second power is defined to be a model second load capacity, whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed.

Claim 82. The supporting system as claimed in claim 71, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein, in said first sequential processes (Jyu: figure 6, sub-numbers 602-612 with column 13, 46-61 and column 14, line 5), informations about gate widths of all p-channel transistors of said constituting gate circuits and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide a gate width of a model p-channel transistor (Jyu: column 9, table 2); informations about gate widths (Jyu: column 9, table 2) of all n-channel transistors of said constituting gate circuits and informations about

currents of basic gate circuits and said constituting gate circuits are utilized to decide a gate width of a model n-channel transistor informations about gate capacities of said all p-channel transistors of said constituting gate circuits and informations about interconnection capacitances between said all p-channel transistors and a first power and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide a model first load capacity (Jyu: columns 13 and 14 lines 65-67 and 1-10 with 60-65, respectively); and informations about gate capacities of said all n-channel transistors of said constituting gate circuits and informations about interconnection capacitances between said all n-channel transistors (Jyu: columns 13 and 14 lines 65-67 and 1-10 with 60-65, respectively; column 9, table 2) and a second power and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide a model second load capacity, whereby said logic gate circuit part comprising at least a pair of p-channel and n-channel transistors and at least a pair of first and second load capacities is designed.

Claim 83. The supporting system as claimed in claim 82, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein a product of the number of said all gate circuits, and a power current ratio of an averaged current value of said basic gate circuits to an averaged current value of said constituting gate circuits, and an averaged value of gate widths of said all p-channel transistors in (Jyu: column 9,

table 2) said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor; a product of the number of said all gate circuits (Jyu: column 11, 1-10), said power current ratio, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor; a product of the number of said all gate circuits, said power current ratio (Jyu: column 17, lines 55-57), and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity; and a product of the number of said all gate circuits, said power current ratio (Jyu: column 17, lines 55-57), and a sum of both a first averaged value of gate capacitances of said all n-channel transistors (Jyu: column 25, lines 1-10 and column 9, table 2) and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity, whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed.

Claim 84. The supporting system as claimed in claim 82, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein a half of a product of the number of said all gate circuits, and a power current ratio (Jyu: column 17, lines 55-57) of an averaged

current value of said basic gate circuits to an averaged current value of said constituting gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor; a half of a product of the number of said all gate circuits, said power current ratio, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor; a half of a product of the number of said all gate circuits, said power current ratio (Jyu: column 17, lines 55-57), and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors (Jyu: column 25, lines 1-10 and column 9, table 2) and said first power is defined to be a model first load capacity; and a half of a product of the number of said all gate circuits, said power current ratio, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity, whereby said logic gate circuit part: comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed.

Claim 85. The supporting system as claimed in claim 71, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein, in said second sequential processes (Jyu:

figure 6, sub-numbers 602-612 with column 13, 46-61 and column 14, line 5), informations about ON-resistances of non-operating-state transistors in said non-operating-state of said constituting gate circuits are utilized to decide an ON-resistance of an equivalent internal capacity; and informations about gate capacities of said non-operating-state transistors in said non-operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state transistors and a power are utilized to decide said equivalent internal capacity, whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

Claim 86. The supporting system as claimed in claim 85, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein a double of a reciprocal of a sum of reciprocals of ON-resistances of non-operating p-channel transistors in said non-operating state is defined to be an ON-resistance of a third equivalent internal capacity; a double of a reciprocal of a sum of reciprocals of ON-resistances of non-operating n-channel transistors (Jyu: column 9, table 2) in said non-operating state is defined to be an ON-resistance of a second equivalent internal capacity; an arithmetic mean of a sum of gate capacities of said non-operating p-channel transistors and a sum of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity; and an arithmetic mean of a sum of gate capacities (Jyu: column

11, lines 1-10 with table 4) of said non-operating n-channel transistors and a sum of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity, whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

Claim 87. The supporting system as claimed in claim 85, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein a double of a product of an averaged value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity; a double of a product (Jyu: column 11, lines 1-10 with table 4) of an averaged value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity; a product of said number of said non-operating gate circuit and an arithmetic mean (Jyu: column 11, lines 1-10 with table 4) of an averaged value of gate capacities of said non-operating p-channel transistors and an averaged value of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity; and a product (Jyu: column 11, lines 1-10 with table 4) of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate

capacities of said non-operating n-channel transistors and an averaged value of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity, whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

Claim 88. The supporting system as claimed in claim 71, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein, in said second sequential processes, informations about an averaged value of ON-resistances of all transistors (Jyu: column 9, table 2) included in said constituting gate circuits and the number of non-operating gate circuits are utilized to decide an ON-resistance of an equivalent internal capacity; and informations about an averaged value of gate capacities (Jyu: column 26, equation 10) of said non-operating-state transistors in said non-operating-state of said constituting gate circuits, and the number of non-operating gate circuits as well as informations about an averaged value of interconnection capacitances between said operating-state transistors and a power are utilized to decide said equivalent internal capacity, whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed (Jyu: column 28, lines 9-36).

Claim 89. The supporting system as claimed in claim 88, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of a total number (Jyu: column 11, lines 1-15 with table 4) of said constituting logic gate included in said semiconductor integrated circuit and a remainder by subtracting an average operational rate from 1; a double of a product (Jyu: column 11, lines 1-15 with table 4) of an averaged value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity; a double of a product (Jyu: column 11, lines 1-15 with table 4) of an averaged value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity; a product of said number(Jyu: column 11, lines 1-15 with table 4) of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating p-channel transistors (column 25, lines 1-18) and an averaged value of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity; and a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating n-channel transistors and an averaged value of

interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity, whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

Claim 90. The supporting system as claimed in claim 88, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of a total number of said constituting logic gate included in said semiconductor integrated circuit and a remainder by subtracting a maximum operational rate from 1; a double of a product of an averaged value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity; a double of a product (Jyu: column 11, lines 1-15 with table 4) of an averaged value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity; a product of said number (Jyu: column 11, lines 1-15 with table 4) of said non-operating gate circuit and an arithmetic mean (Jyu: column 11, table 4) of an averaged value of gate capacities of said non-operating p-channel transistors and an averaged value of interconnection capacities between said non-operating p-channel transistors and a

first power is defined to be said second equivalent internal capacity; and a product of said number (Jyu: column 11, lines 1-15 with table 4) of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating n-channel (Jyu: column 25, lines 1-18) transistors and an averaged value of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity, whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

Claim 91. The supporting system as claimed in claim 71, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein informations about an averaged value of ON-resistances of all transistors included in said constituting gate circuits and informations about currents of basic gate circuits (Jyu: column 9, table 2) and said constituting gate circuits are utilized to decide an ON-resistance of an equivalent internal capacity; and informations about an averaged value (Jyu: column 25, lines 1-18) of gate capacities of said non-operating-state transistors in said non-operating-state of said constituting gate circuits, and informations about currents of basic gate circuits and said constituting gate circuits as well as informations about an averaged value of interconnection capacitances between said operating-state transistors and a power (Jyu: column 14, lines 60-65) are utilized to decide said equivalent internal capacity, whereby said equivalent

internal capacitive part comprising at least said equivalent internal capacity is designed.

Claim 92.The supporting system as claimed in claim 91, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of the total number (Jyu: column 11, lines 1-11) of the constituting gate circuits included in the semiconductor integrated circuit and a power current ratio which is defined to be a ratio of an averaged current value of all of basic gate circuits to an averaged current value of all of the constituting gate circuits; a double of a product of an averaged value of ON-resistances of non-operating p-channel transistors (Jyu: column 25 ,lines 1-18) in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity; a double of a product (Jyu: column table 4) of an averaged value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity; a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating p-channel transistors and an averaged value of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent

internal capacity; and a product of(Jyu: column table 4) said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating n-channel transistors and an averaged value of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity, whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

Claim 93.The supporting system as claimed in claim 71, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein said equivalent internal capacitive part (Jyu: column 13 and 14, lines 65-67 and 1-10, respectively) is placed between said logic gate circuit part and a power system side (Jyu: column 14, lines 60-67).

Claim 94. The supporting system as claimed in claim 71, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein said power model is deigned for simulation to a current distribution over a circuit board on which said semiconductor integrated circuit is mounted (EIAJ: pg. 11-12, section 5.2.5, Pad Assignment).

Claim 95. The supporting system as claimed in claim 94, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein said power model is deigned for an electromagnetic interference simulation (EIAJ: pg. 2, Outline, part 7) to an electromagnetic field distribution over a circuit board on which said semiconductor integrated circuit is mounted (EIAJ: pg. 11-12, section 5.2.5, Pad Assignment).

Claim 96. The supporting system as claimed in claim 71, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein said computer program further includes a first simulation program for analysis to circuits.

Claim 97. The supporting system as claimed in claim 96, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with figure 1; column 11, lines 37-39) wherein said first simulation program is to obtain a current (EIAJ: pg. 13, line 12) distribution over a circuit board on which said semiconductor integrated circuit is mounted (EIAJ: pg. 11-12, section 5.2.5, Pad Assignment).

Claim 98. The supporting system as claimed in claim 97, (EIAJ: pg.1, Background, pg. 2, Outline, pg. 11-12, section 5.2.5; Jyu: abstract: Jyu: column 4, lines 1-5 with

figure 1; column 11, lines 37-39) wherein said computer program further more includes a second simulation program for analysis (Jyu: column 14, line 62) to electromagnetic field to obtain a distribution of electromagnetic field over said circuit board on which said semiconductor integrated circuit is mounted (EIAJ: pg. 11-12, section 5.2.5, Pad Assignment).

Claim 99. A simulator for simulating an electro-magnetic interference (EIAJ: pg. 2, Outline), said simulator comprising a circuit analyzing simulator being accessible to a first storage medium for receiving a power model (Jyu: abstract) for a semiconductor integrated circuit, and also being connected to a second storage medium for receiving informations about a circuit board (Jyu: column 5, line 61) on which said semiconductor integrated circuit is mounted (EIAJ: pg. 11-12, section 5.2.5, Pad Assignment), so that said circuit analyzing simulator analyzes said power model to obtain a current distribution over a circuit board on which said semiconductor integrated circuit is mounted ; an electromagnetic field analyzing simulator being accessible to said circuit analyzing simulator for receiving said current (EIAJ: pg. 13, line 12) distribution, so that said electromagnetic field analyzing simulator analyzes an electromagnetic field distribution over said circuit board on which said semiconductor integrated circuit is mounted, wherein said power model comprises a logic gate circuit part representing an operating part of said semiconductor integrated circuit and an equivalent internal capacitive part representing a non-operating part of said semiconductor integrated circuit.

Claim 100. The simulator as claimed in claim 99, (EIAJ: pg. 2, Outline, pg. 11-12, section 5.2.5, Pad Assignment; Jyu: abstract) wherein said power model is independently provided for each of plural power systems which are independent from each other (EIAJ: pg. 2, figure 3.1) and included in said semiconductor integrated circuit.

Claim 101. The simulator as claimed in claim 99, (EIAJ: pg. 2, Outline, pg. 11-12, section 5.2.5, Pad Assignment; Jyu: abstract) wherein internal circuit configurations of said semiconductor integrated circuit are divided into plural blocks on the basis of arrangement informations (EIAJ: pg. 3, Model Structures) and said power model is provided for each of said plural blocks.

Claim 102. The simulator as claimed in claim 99, (EIAJ: pg. 2, Outline, pg. 11-12, section 5.2.5, Pad Assignment; Jyu: abstract) wherein internal circuit configurations of said semiconductor integrated circuit are divided into plural groups (EIAJ: pg. 3, Model Structures), each of said plural groups comprises a same timing group which includes logic gate circuits having individual signal transmission delay times (Jyu: column 32, lines 25-26) fallen in a group-belonging predetermined time range which belongs to each of said plural groups, and said power model is provided for each of said plural groups.

Claim 103. The simulator as claimed in claim 99, (EIAJ: pg. 2, Outline, pg. 11-12, section 5.2.5, Pad Assignment; Jyu: abstract) wherein said power model further comprises a signal source connected to said logic gate circuit part for supplying a frequency-fixed signal (Jyu: column 2, line 6) to said logic gate circuit part, so that said logic gate circuit part represents operating state parts of said semiconductor integrated circuit in accordance with said frequency-fixed signal (Jyu: column 2, line 6), and said equivalent internal capacitive (Jyu: column 21, lines 64-66) part represents non-operating state parts of said semiconductor integrated circuit.

Claim 104. The simulator as claimed in claim 103, (EIAJ: pg. 2, Outline, pg. 11-12, section 5.2.5, Pad Assignment; Jyu: abstract) wherein said equivalent internal capacitive (Jyu: column 21, lines 64-66) part further represents operating-irrelevant fixed parts of said semiconductor integrated circuit.

Claim 105. The simulator as claimed in claim 104, (EIAJ: pg. 2, Outline, pg. 11-12, section 5.2.5, Pad Assignment; Jyu: abstract) wherein said logic gate circuit part is connected between first and second powers, and said equivalent internal capacitive part is also connected between said first and second powers.

Claim 106. The simulator as claimed in claim 105, (EIAJ: pg. 2, Outline, pg. 11-12, section 5.2.5, Pad Assignment; Jyu: abstract) wherein said logic gate circuit part further comprises a single pair of an inverter circuit (Jyu: column 27, lines 30-

32) and a load capacitive element, and said inverter circuit is connected between said first and second powers and said load capacitive element is also connected between said first and second powers (EIAJ: pg. 16, figure 5.3, V_{cc2} and V_{cc3}), and said load capacitive element is placed between said inverter circuit (Jyu: column 27, lines 30-32) and said equivalent internal capacitive part.

Claim 107. The simulator as claimed in claim 106, (EIAJ: pg. 2, Outline, pg. 11-12, section 5.2.5, Pad Assignment; Jyu: abstract) wherein said load capacitive element comprises a series connection of a first load capacitance and a second load capacitance between said first and second powers (EIAJ: pg. 16, figure 5.3, V_{cc2} and V_{cc3}), and an intermediate point between said first and second load capacitances (Jyu: column 14, table 5, point 6) is connected to an output terminal of said inverter circuit.

Claim 108. The simulator as claimed in claim 107 (EIAJ: pg. 2, Outline, pg. 11-12, section 5.2.5, Pad Assignment; Jyu: abstract), wherein said equivalent internal capacitive part further comprises at least an equivalent internal capacitive (Jyu: column 21, lines 64-66) element connected between said first and second powers (EIAJ: pg. 16, figure 5.3, V_{cc2} and V_{cc3}).

Claim 109. The simulator as claimed in claim 108, (EIAJ: pg. 2, Outline, pg. 11-12, section 5.2.5, Pad Assignment; Jyu: abstract) wherein a plurality of said equivalent

internal capacitive element (Jyu: column 21, lines 64-66) is connected between said first and second powers, and said equivalent internal capacitive element comprises a series connection of a capacitance and a resistance between said first and second powers (EIAJ: pg. 16, figure 5.3, V_{cc2} and V_{cc3}).

Claim 110. The simulator as claimed in claim 109, (EIAJ: pg. 2, Outline, pg. 11-12, section 5.2.5, Pad Assignment; Jyu: abstract) wherein said inverter circuit comprises (Jyu: column 27, lines 30-32) a series connection of a p-channel MOS field effect transistor (Jyu: column 6, lines 10-15; and column 9, table 2; EIAJ: pg. 19, part (ii) through pg. 21, specifically figures 5.6) and an n-channel MOS field effect transistor, and gate electrodes of said p-channel and n-channel MOS field effect transistors are connected to a clock signal source for applying a clock signal to said gate electrodes of said p-channel and n-channel MOS field effect transistors.

Claim 111. The simulator as claimed in claim 105, (EIAJ: pg. 2, Outline, pg. 11-12, section 5.2.5, Pad Assignment; Jyu: abstract) wherein said logic gate circuit part further comprises plural pairs of an inverter circuit (Jyu: column 27, lines 30-32) and a load capacitive element, and said inverter circuit is connected between said first and second powers (EIAJ: pg. 16, figure 5.3, V_{cc2} and V_{cc3}) and said load capacitive element is also connected between said first and second powers, and

in each pair; said load capacitive element is placed closer to said equivalent internal capacitive (Jyu: column 28, lines 9-36) part than said inverter circuit.

Claim 112. The simulator as claimed in claim 111, (EIAJ: pg. 2, Outline, pg. 11-12, section 5.2.5, Pad Assignment; Jyu: abstract) wherein said load capacitive element comprises a series connection of a first load capacitance and a second load capacitance between said first and second powers (EIAJ: pg. 16, figure 5.3, V_{cc2} and V_{cc3}), and an intermediate point between (Jyu: column 14, lines 60-67) said first and second load capacitances is connected to an output terminal of said inverter circuit.

Claim 113. The simulator as claimed in claim 112, (EIAJ: pg. 2, Outline, pg. 11-12, section 5.2.5, Pad Assignment; Jyu: abstract) wherein said equivalent internal capacitive part further comprises at least an equivalent internal capacitive element (Jyu: column 21, lines 60-67) connected between said first and second powers (EIAJ: pg. 16, figure 5.3, V_{cc2} and V_{cc3}).

Claim 114. The simulator as claimed in claim 113, (EIAJ: pg. 2, Outline, pg. 11-12, section 5.2.5, Pad Assignment; Jyu: abstract) wherein a plurality of said equivalent internal capacitive element (Jyu: column 21, lines 60-67) is connected between said first and second powers, and said equivalent internal capacitive element comprises a series connection of a capacitance and a resistance (Jyu:

column 14, table 5, point 6) between said first and second powers (EIAJ: pg. 16, figure 5.3, V_{cc2} and V_{cc3})

Claim 115. The simulator as claimed in claim 114, (EIAJ: pg. 2, Outline, pg. 11-12, section 5.2.5, Pad Assignment; Jyu: abstract) wherein said inverter circuit comprises a series connection of a p-channel MOS field effect transistor and an n-channel MOS field effect transistor (Jyu: column 6, lines 10-15; and column 9, table 2; EIAJ: pg. 19, part (ii) through pg. 21, specifically figures 5.6), and gate electrodes of said p-channel and n-channel MOS field effect transistors are connected to a clock signal source for applying a clock signal (Jyu: column 2, line 6) to said gate electrodes of said p-channel and n-channel MOS field effect transistors.

Claim 116. The simulator as claimed in claim 99, (EIAJ: pg. 2, Outline, pg. 11-12, section 5.2.5, Pad Assignment; Jyu: abstract) wherein said equivalent internal capacitive part (Jyu: column 21, lines 60-67) is placed between said logic gate circuit part and a power system side (Jyu: column 20, line 14).

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is (703) 305-

0365, Monday-Friday (8:00 am- 4:30 pm) or contact Supervisor Mr. Kevin Teska at (703) 305-9704. The fax number for the group is 703-872-9306.

Any inquires of general nature or relating to the status of this application should be directed to the Group receptionist whose phone number is (703) 305-3900.

September 27, 2004

THS

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER